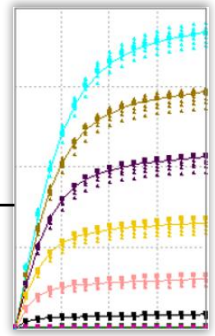
Recalibration of MOSFET Compact Models based on Complex Product-Related Layouts using Bayesian Optimization

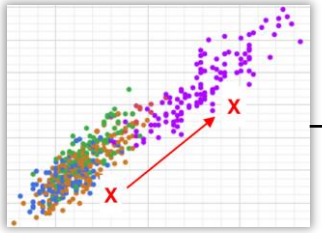
Lan Luo, David Winston, Robert Perricone, Bria Matthews and Richard Wachnik
IBM Infrastructure

SPONSORED BY

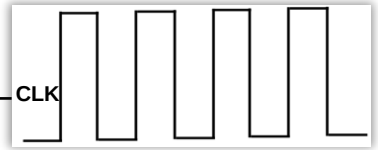
Technology Evolution Drives MOSFETs Model Recalibration

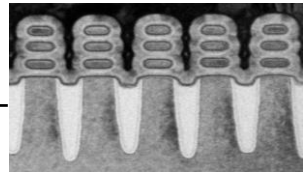
- Physics-based model equations [1]
- Many model parameters
- I-V, C-V, noise and RF datasets
- Period of weeks to months





- Limited model parameters
- Discrete parametric targets
- Period of days to weeks





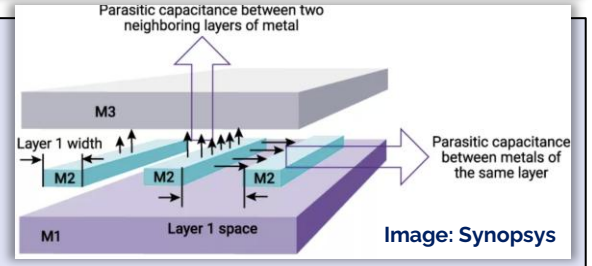
IBM Nanosheet, EE Times 2017

Device fabrication → Device Asfit Modeling → Device model recalibration → Circuit SPICE simulation

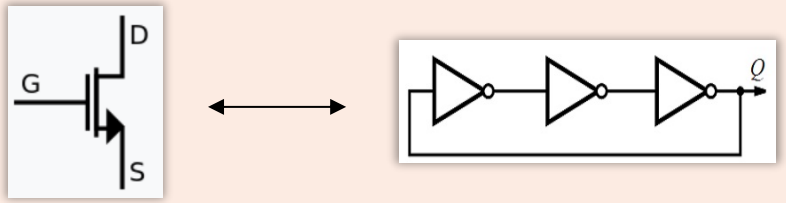
[1] Girish Pahwa, et al., "BSIM-CMG 111.2.1: Multi-Gate MOSFET Compact Model," University of California, Berkeley, 2022

Technology Scaling Challenges Model Recalibration

- Challenges to accurate MOSFET modeling arise from:
  - Increasing wiring parasitic.
  - Increasing Local Layout Effect (LLE).
  - Increasing SPICE simulation time from accurate Parasitic EXtraction (***PEX***) netlists



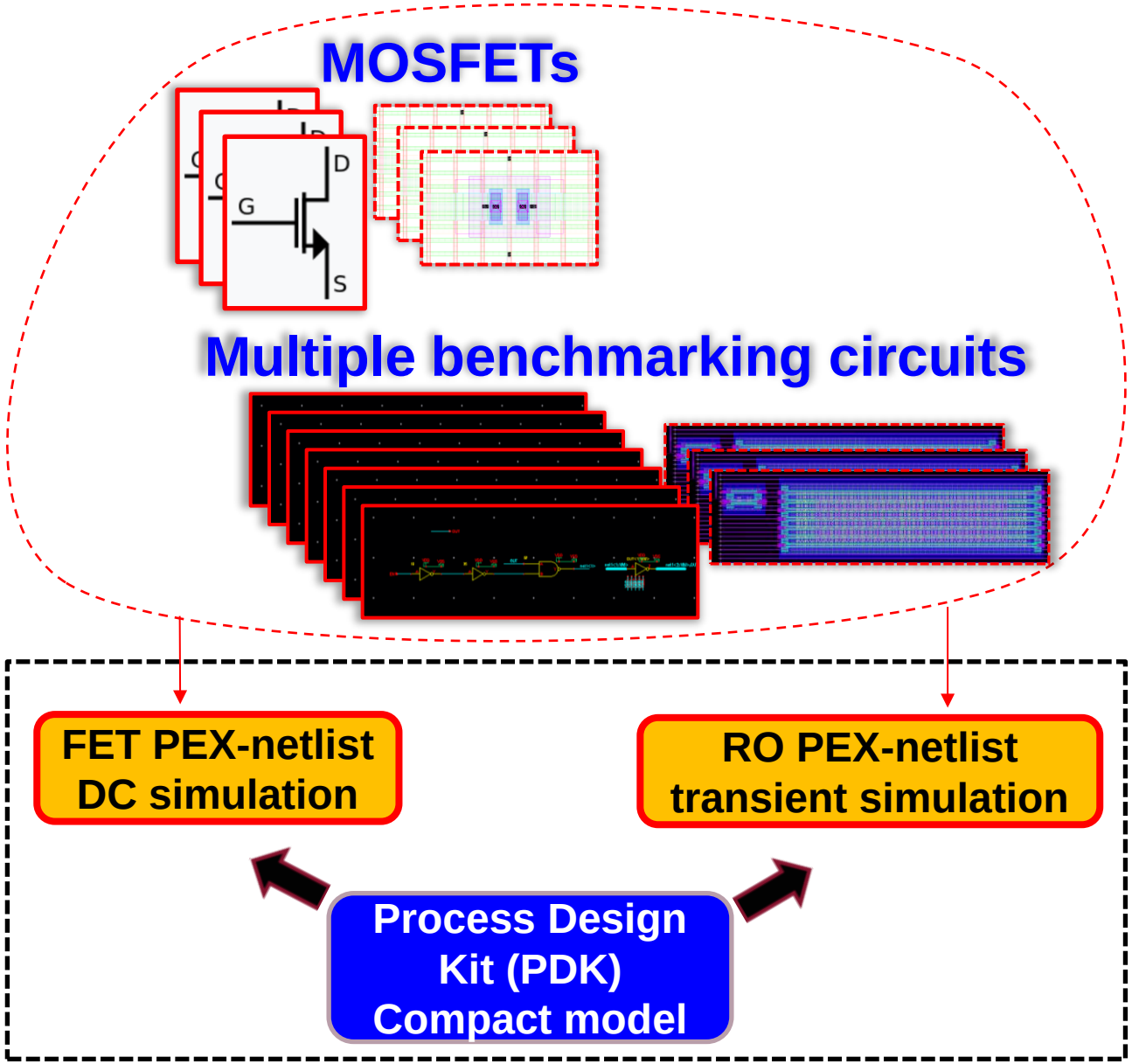
- Discrepancy between ***product circuit*** measurement and SPICE simulation, which is based on ***single device*** extrapolated compact model:
  - operating under different PVT conditions.
  - surrounded with different layout environments.
  - optimized with different performance targets.



Most prior arts only support device-level model recalibration based on simplified pre-layout schematic netlist [2][3].

[2] Sachin Bhat, *et al*., "Compact Model Parameter Extraction using Bayesian Machine Learning," IEEE Computer Society Annual Symposium on VLSI, 2023
[3] Jeesoo Chang, et al., "A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm," Applied Sciences (2076-3417), 2021, Vol 11, Issue 9, p4155

Main idea #1: Multiple Product-Related Layouts Driven Recalibration



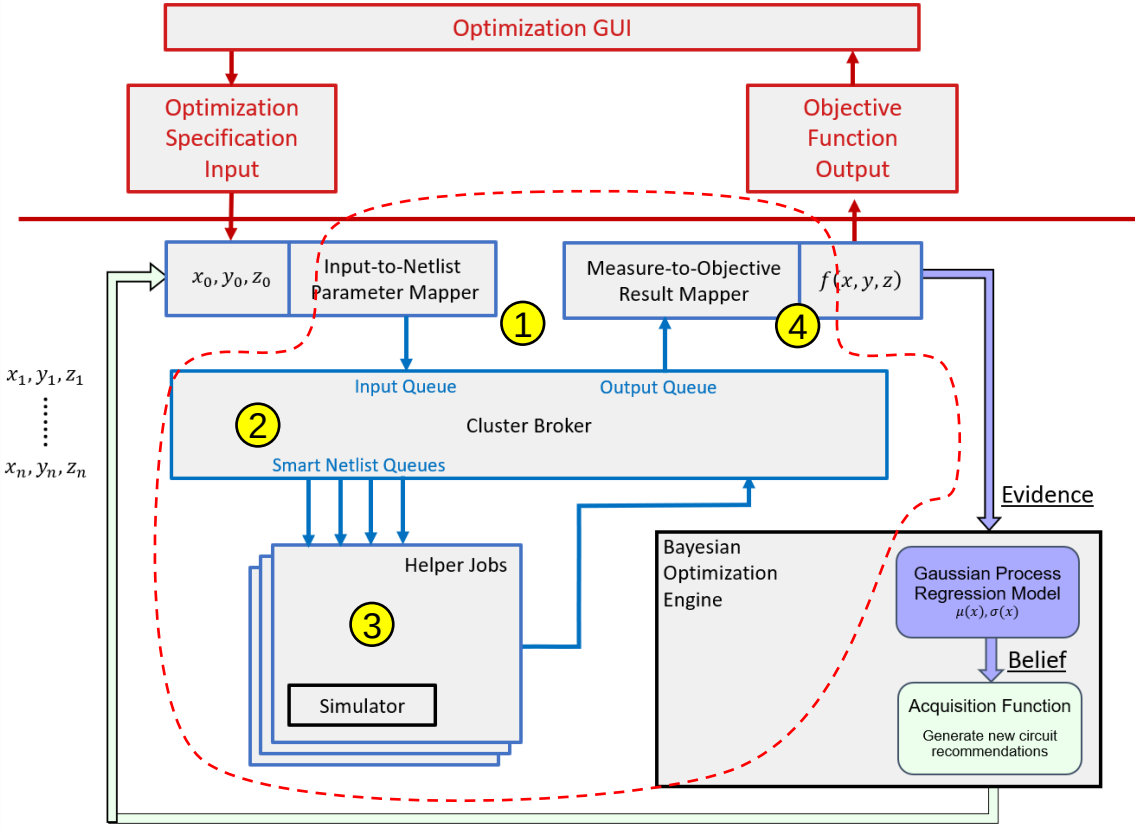
- ***Multiple*** product performance benchmarking circuits are included to drive model recalibration.
  - Ring oscillator (RO) ↔ combinational logic circuit
  - LATCH ↔ sequential logic circuit
  - SRAM ↔ array structures
  - current mirror ↔ analog module
- ***PEX***-netlists based SPICE simulation for both benchmarking circuits and devices.

Multi-circuit optimization problem!

Main idea #2: In-Parallel Multi-Circuit Bayesian Optimization

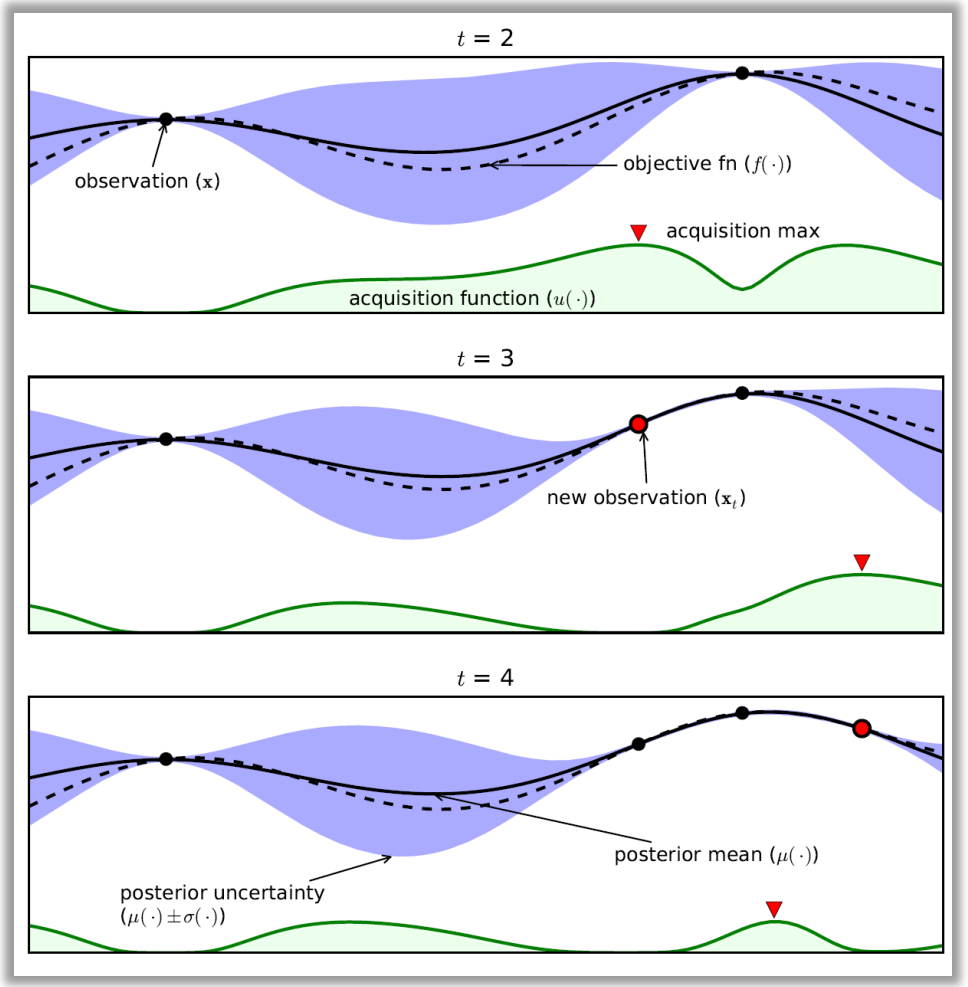
A parallel Bayesian optimization algorithm and associated software infrastructure to solve multi-circuit optimization.

1. ***Input-to-Netlist Parameter Mapper***
   - Maps one or more “optimization parameters” to one or more “netlist parameters”
   - Defines bounds, step size, constraints
2. ***Cluster Broker***
   - Launches multiple simulator “helper” jobs
   - Maintains smart queues to maximize the parallelism
3. ***Helper Jobs***
   - Can rerun existing simulation with new optimization parameters
   - Restart simulation on different netlist if required
4. ***Measure-to-Objective Result Mapper***
   - Collects outputs from individual simulation and constructs objective function



Why Choose Bayesian Optimization

- Bayesian Optimization is an efficient global optimization strategy for:
  - expensive black box function: **multi-circuit PEX netlist SPICE simulations**.
  - optimization with a limited optimization parameters: **limited model parameters for recalibration**.
  - searching the global min/max for objective function: **SPICE simulation vs. hardware targets**.
- Two Key Components:
  - Surrogate Function: Statistical model built from a Gaussian Process Regression using the training data.
  - Acquisition Function: Function to determine next position to sample.

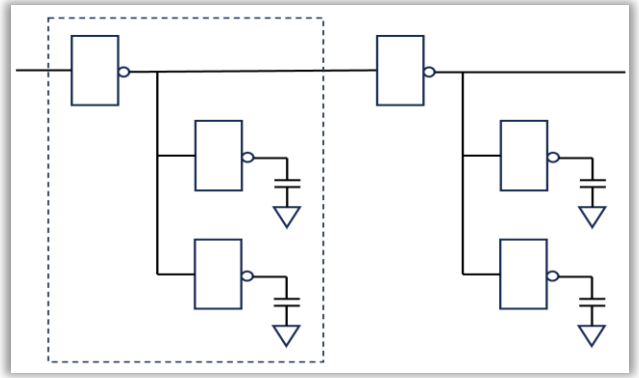


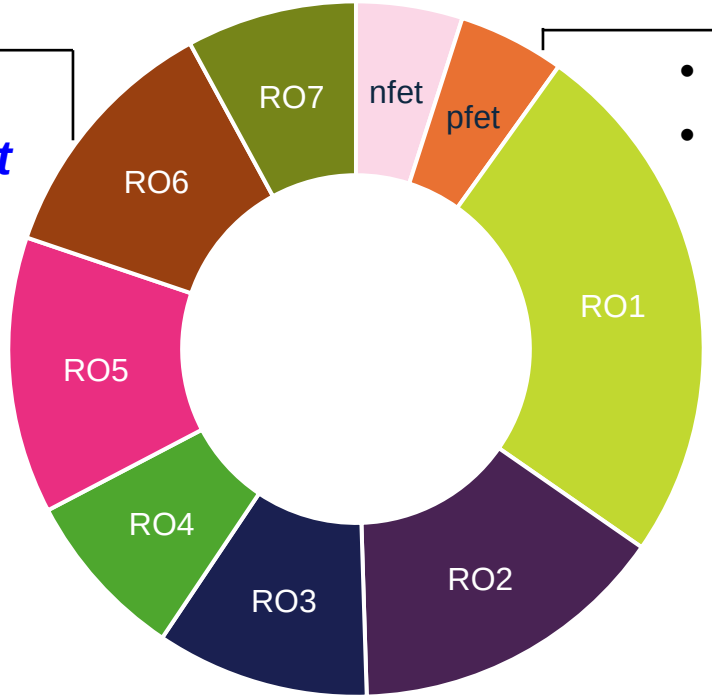
[4] E. Brochu, *et al*. "A tutorial on Bayesian optimization of expensive cost functions, with application to active user modeling and hierarchical reinforcement learning," *arXiv:1012.2599*, 2010.

A Practical Example

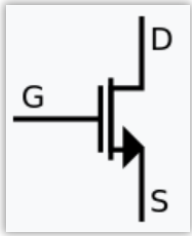
- ❑ **A MOSFET model recalibration based on a multi-Vt FinFET technology.**
- ❑ **Model recalibration combining DC analysis on *single transistor devices* (n and p) and transient analysis on *multiple ring oscillator (RO) circuits*.**
  - ❑ **101-stage RO**
  - ❑ **Different NOT gate type: INV, NAND, NOR, …**

- **PVT**: product use corners
- **Circuit analyses**: ***multiple transient simulation netlist***





- **PVT**: nominal corner
- **Circuit analyses**: ***one DC simulation netlist***



Practical Example Continues

How to formulate objective function?

- Evaluation metrics are the combination of 7 ROs and 2 FETs.
  - MOSFET: threshold voltage ***Vt*** and effective current ***Ieff***
  - RO: ***frequency***
- A "global" RO is defined to represent the overall performance of multiple ROs.
  - $W1_j$: weight factor for each RO
  - $Freq_j$: frequency metric of each RO

$$RO\_Freq_g = \sum_{j=1}^{7} W1_j * Freq_j$$

- Normalized unitless error "Err_i" is defined for each individual metric
  - opt_i: recalibrated model simulation result
  - tgt_i: target extracted from hardware measurement

$$Err_i = \frac{(opt_i - tgt_i)^2}{tgt_i^2}$$

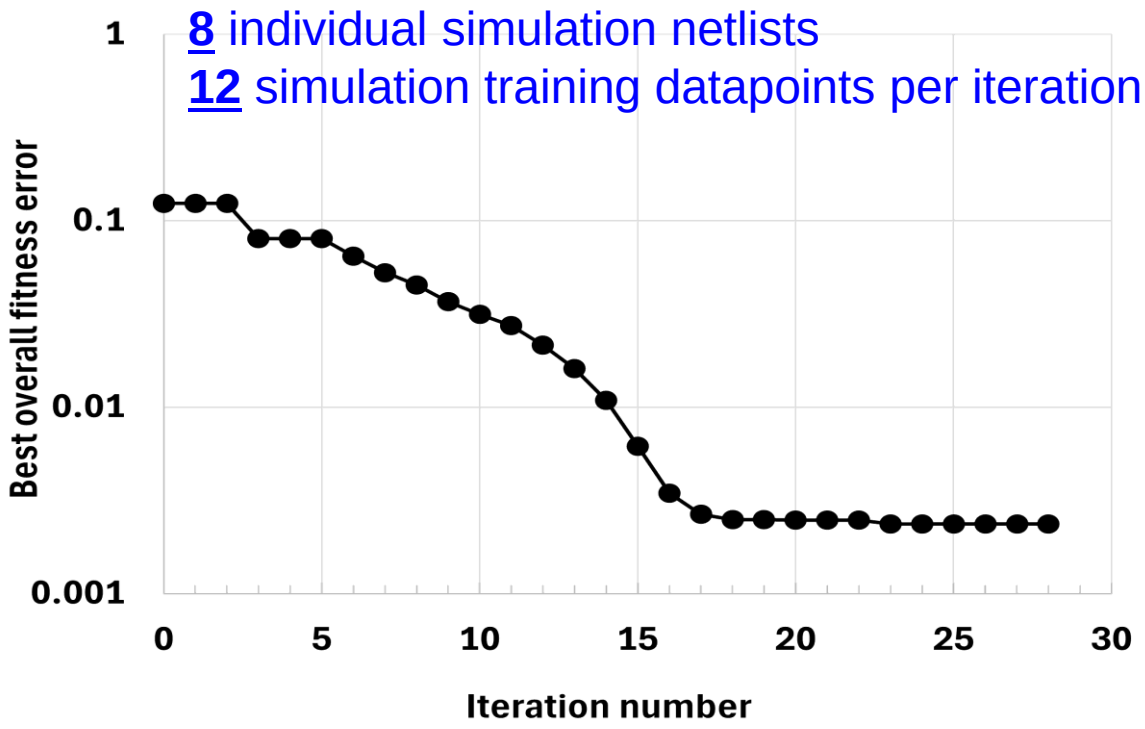
- Total ***fitness error score*** is the sum of normalized unitless errors.
  - $W2_i$: weight factor of individual metric (frequency/Vt/Ieff)

$$Fitness\_err = \sum_{i=1}^{N} W2_i * Err_i$$

❑ ***~10 BSIM-CMG model parameters selected:***

- **Work function parameters**
- **Mobility parameters**
- **Capacitance parameters**
- **Local layout effect parameters**

Results



	Manual recalibration	Auto-recalibration
Metrics	**Model vs. target**	**Model vs. target**
Vt (NFET)	-1.71 mV	-0.12 mV
Ieff (NFET)	2.10%	-0.76%
Vt (PFET)	0.57 mV	-0.09 mV
Ieff (PFET)	2.38%	0.20%
Freq (RO1)	2.39%	0.05%
Freq (RO2)	-5.66%	-3.72%
Freq (RO3)	-2.37%	-0.33%
Freq (RO4)	-3.48%	-0.70%
Freq (RO5)	1.17%	3.98%
Freq (RO6)	1.55%	-0.43%
Freq (RO7)	3.40%	1.38%
RO_Freq_g	0.53%	0.03%
Time	**~ 1 human week**	**~ 32 machine hrs.**

- ***96*** simulations per iteration distributed in ***24*** machines in-parallel .
- Best score found in iteration ***#23*** with total 288 (=24*12) training datapoints.
- Total turnaround time is ***~ 32 hours***.

- **The turnaround time of manual recalibration is very dependent on the skill of the model engineer.**
- **With our multi-design circuit Bayesian optimization infrastructure, turn-around-time has been reduced *from weeks to days or hours with better model quality*.**

Summary

- ***Improved accuracy*** through MOSFET model recalibration:
  - Leveraging ***multiple product-related circuits*** to drive model recalibration.
  - Including ***Parasitic EXtraction netlist*** in SPICE simulation.

- ***Enhanced efficiency*** of MOSFET model recalibration:
  - utilizing ***Bayesian optimization*** algorithm.
  - developing ***multi-circuit optimization*** infrastructure.

- Demonstrated reduction of turn-around-time from weeks to days with better model quality.